Compact Low Power Avionics for the Europa Lander Concept and Other Missions to Ocean Worlds

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Abstract— **This paper presents the results of NASA's Game Changing Technology development entitled "Ultra Low Temperature Electronics" and ColdTech technology effort entitled "Cold Survivable Distributed Motor Controller". The purpose of these back-to-back projects is to address the Command & Data Handling (CDH), Power and Motor Control needs for missions to ocean worlds such as the potential Europa Lander project. We addressed the mass reduction challenge by developing the key technologies necessary to design a next generation compact motor control avionics. The project's goal is to allow a Europa Lander to last longer on the surface and provide more room for additional science by reducing the volume, mass and power of its avionics and the amount of energy required to keep the avionics warm.**

Keywords-component; Low Temperature Electronics; Europa Lander; Custom SiP Multi-Chip Modules; Radiation Tolerant

I.   INTRODUCTION

Potential Ocean World missions, whether looking for extant life, sample acquisitions, or ocean access, share a common need of reducing the size, weight and power (SWaP), for their spacecraft and electronics. Our proposed modular approach targeted for centralized or distributed actuator and control electronics significantly reduces the cost, mass, and complexity of these electronics systems as compared to previous systems deployed on MSL, Mars 2020, MER, and Phoenix. Reducing SWaP enables more science return by allowing room for additional instruments, or added mission life by allowing more mass for batteries.

Landed payload mass of Ocean World mission concepts typically require a spacecraft launch mass of 7-10x the landed mass due to the required propellant to get payload to the surface. We address the mass requirement by developing modular standardized Custom SiP Multi-Chip Modules (MCMs). These custom MCM's utilizing advanced substrate and System-in-Package (SiP) technologies that can be configured into a compact yet versatile avionics topology that significantly reduces SWaP over previously flown avionics assemblies.

This technology allows for a decrease in the volume (10x), and mass (3x), and reduces the power (2x) by the use of an efficient processor and on-board power management. The energy required to keep the electronics warm is reduced by allowing the electronics to be stored at the ambient environment and heated prior to operation.

Our technology has benefits, beyond distributed motor control. This technology is applicable to any electronic assembly that needs to be housed in an external environment. This may include instruments electronics, controllers and cameras. The modules we have developed are designed to be 300Krad tolerant, meeting the needs of potential Europa missions. We have developed modules with a goal to make them standardized products. For example, our 300Krad hard isolated converters and point-of-load regulators are common needs across many missions.

This work was divided into the following major thrust areas: Advanced Electronic Packaging, Low Power Computing, and Cold Capable Electronics. The results of this work were:

1. Advanced Electronic Packaging (Key modules for a 3U Motor Controller Card)
2. Low Power Computing (Single Board Command and Data Handling System)
3. Cold Survivable Electronics (Eliminates the need for survival heating)
4. SiP Module level radiation shielding for extreme radiation environment applications.

II.   PROJECT GOAL

The project's goal is to reduce the volume, mass and power of its avionics and the amount of energy required to keep the avionics warm. The effort to date has achieved its project goal through the use of advanced electronic packaging, low power computing and cold capable electronics, as illustrated in Table 1. The energy required to keep the electronics warm is reduced by allowing the electronics to be stored at the ambient environment and

heated prior to operation. As illustrated in Table 2 the power required for survival heating is eliminated.

Baseline Lander Avionics		
Mass	14.13	Kg
Volume	11250	cc
Power	26	W

Tech Lander Avionics		
Mass	3.58	Kg
Volume	1159	cc
Power	13.44	W

Table 1: Compact Ultra Low Temperature Electronics Goal

Baseline Lander Avionics		
Surviaval	-55C to	+70C

Tech Lander Avionics		
Surviaval	-200C to	+70C

Table 2: Survival Temperature Goal

The benefits to the Europa Lander concept would be decreased mass, volume and power required for heating of the electronics. The benefits include increased science return, lower mission cost and improved reliability. Science return would be increased through the decrease in volume of the electronics allowing for more room for science instruments. The decrease in power of the electronics would allow the lander to last longer on the surface. Mission costs is addressed by eliminating the need for survival heaters on the surface and on the long transit to the Europa surface. Reliability is improved through the mass and volume reduction by freeing up space for a dual string system.

III. SYSTEM ARCHITECTURE

Actuator control is a common need across missions to the ocean worlds of the outer Solar System (e.g., Enceladus, Europa, and Titan). Actuators are used for many purposes including antenna pointing, or drilling and scooping for sample collection and handling. The current Europa Lander concept requires at least 12 actuators. The Cryobot, a mission concept aimed at reaching Europa's oceans, would require actuators for sample collection and handling, and motors for water pumps used for control. A long-reach robotic arm is being planned to address the needs of missions beyond the current Europa Lander design. The reduction in cable and electronics mass of a distributed design would allow this arm to be much lighter and more flexible than it would be if all the cabling for the actuators had to be routed from a centralized location through the arm.

Beyond actuator control, these techniques can be applied to distributed power switching and conversion, and instrument control. We will be focusing on actuator control for our demonstration because it has all the challenges of our proposed applications.

A. Solution

Placing the control and power conversion electronics at or near the actuators/instruments is the key change that lies at the core of our proposed distributed architecture. We intend to do this by developing the technology necessary to distribute the electronics, placing them on a shared interface and power bus. This allows for significant reduction in cable mass along with a reduction in complexity. It also allows spacecraft designers to take advantage of volume at the extremities that would not be utilized normally.
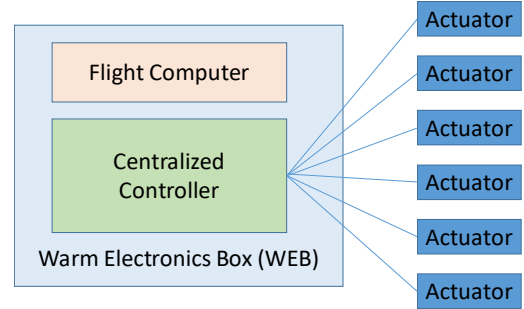

Figure 1(a): Current state a practice: Point to point wiring
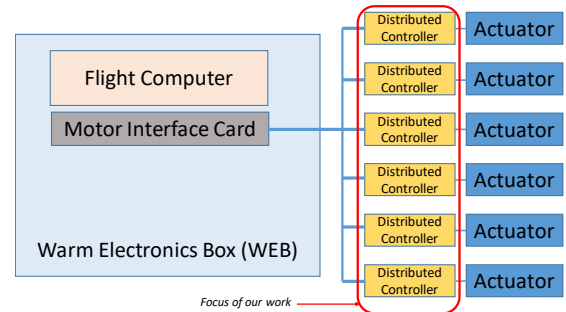

Figure 1(b) Proposed: Distributed Motor Control

Conventional warm electronics box (WEB)-based actuator control systems are highly complex, using point-to-point wiring to connect the drive and control electronics to motors usually located at the system appendages (~2000 wires for a small rover like MER). Our proposed technology minimizes the dependency of the motor controller on the WEB, eliminates the point-to-point wiring, and reduces the wire count tremendously with concomitant savings in mass. A key challenge for this technology is to be able to survive the ambient environment. On Europa, the temperature can be as cold as -180°C. Our electronics are designed to survive at least 100 cycles from -180°C to +85°C.

B. Addressing the Challenge

The use of a new advanced packaging technology will enable us to meet our objectives. This technology meets these requirements by combining JPL's expertise in cold capable electronics; packaging and power conversion together with the i3's CoreEZ® high density interconnect technology. The combination has resulted in a unique high-density technology that allows for decreased SWaP actuator/motor controllers capable of surviving cold world environments.
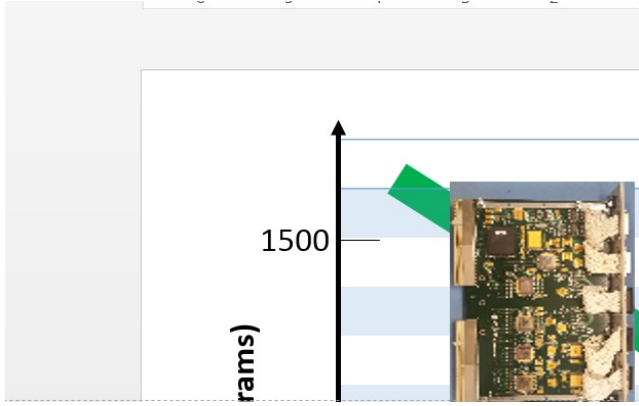
Figure 2: Motor Resolver Electronics

Figure 2 is an illustration of the relative size of a conventionally packaged board (10cm x 15cm) to the same electronics packaged using the proposed advanced packaging technology (2.5cm x 2.5cm).

IV. ENABLING TECHNOLOGY

The substrate technology selected is the key enabler towards board density reduction. CoreEZ [1,2,3] a high-density substrate fabricated from thin particles containing organic laminates was the alternative to standard PWBs that contain glass cloth reinforced dielectrics..

Figure 3 shows a cross-section comparison of silica particle filled epoxy-based CoreEZ thin laminate compared to a standard build up PWB. The absence of glass cloth in the dielectric provides several distinct key advantages including; reduction in thickness, tighter core via pitch, and improvements in assembly yields and reliability. It also results in a smoother surface finish on the particle-filled dielectric, enabling higher resolution photolithography for finer line widths and spaces, and improved electrical performance, especially for high-speed applications.
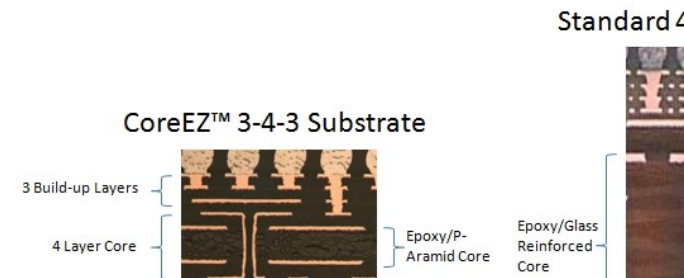

Figure 3: Photographs comparing CoreEZ MCM technology and standard PWB technologies.

A. Reliability – Lower Temperature Exposer

Understanding reliability for extreme applications can be validated through stress testing, which has numerous advantages that extend beyond the scope of this paper. However, understanding key attributes, especially related to substrate properties and configuration over low temperatures would be very informative for our goals.

Production coupons or "Current Induced Thermal Cycle" (CITC's) coupons [4,5,6] were used to characterize the substrate technology for low temperature survivability. Figure 4 shows a typical CITC's coupon sample configured for thermal cycling. This sample was wirebonded to an open cavity test package and wired to monitor resistance changes over temperature.
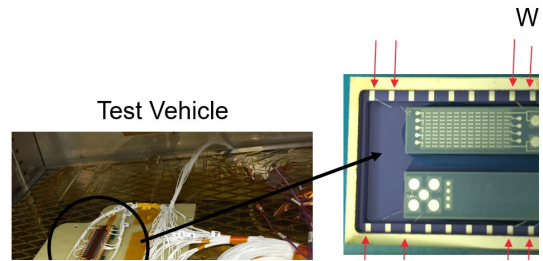

Figure 4. Photographs illustrating the CITC sample preparation.

The CITC test vehicle was exposed to the following temperature schedule: from 25°C to 0°C to -50°C to -100°C to 150°C to -180°C back to 25°C with a 15 min dwell at each temperature and a 20 min dwell at -180°C. Figure 5 shows resistance trend with temperature, providing an early assessment of substrate behavior as a function of temperature to -180°C.
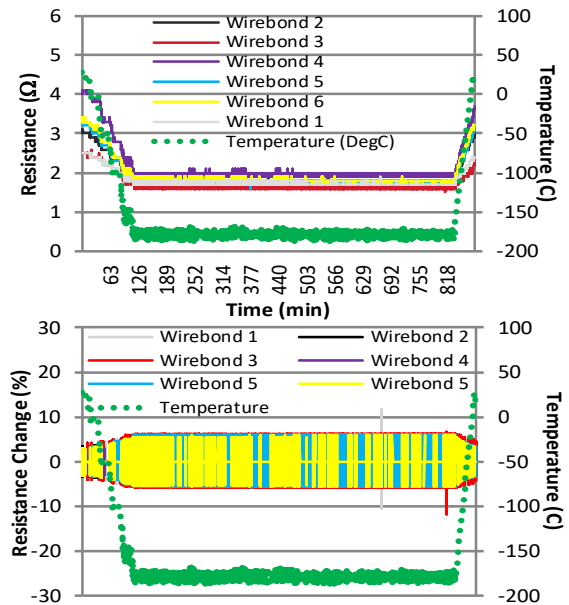

Figure 5. Plots of CITC sample (a) resistance with temperature and (b) percent resistance change (compared to room temperature value) with temperature.

Our single CITC's sample with a 3-4-3 stackup, representative of the current module designs have shown positive result. Future plans and fabrication are underway to

perform additional qualification tests, using daisy chain CITC's array to further validate low temperature performance.

B. Reliability – Radiation Exposure

CoreEZ laminate structure was evaluated to various radiation levels in a previous work [7]. Structures were exposed to radiation dosage using Cobalt-60 Gamma spectrum from 32 up to 5000 krad Total Ionizing Dose (TID). Figure 6 shows testing results of substrate materials indicate no radiation induced degradation, or change in ductility performance, indicating material performance is not expected to degrade even in relatively sever radiation environments,
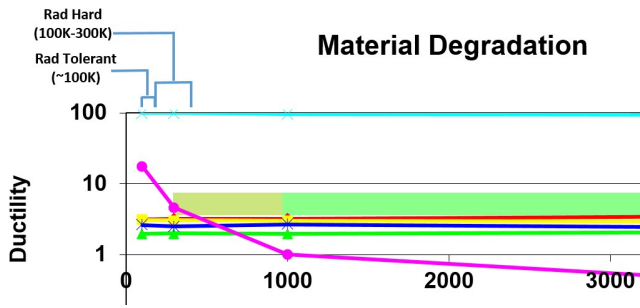

Figure 6. CoreEZ exposure to radiation dosage

V. MINIATURIZED MOTOR CONTROLLER TOPOLOGY

Motor control requires four basic functions as shown in Figure 7, Motor Drive, Current Sense (ADC & Signal processing), Commutation (resolvers) and Power Conversion. Focusing on key electronic functions and modern system in package technologies provides for "modular user-optional" solutions for a distributed or centralized solution.

In the case for Cold Survivable Distributed Motor Controller (CSDMC), will be built using a MCM based approach that builds upon prior work. Our proposed architecture divides motor control between the warm box computer, which performs all mission dependent functions including control loop closure and associated algorithms, and the cold module that performs motor and sensor interface, analog/digital conversion, and commutation. This architecture minimizes the number of complex components residing in the cold module, thus minimizing cold module mass, volume, cost and risk.
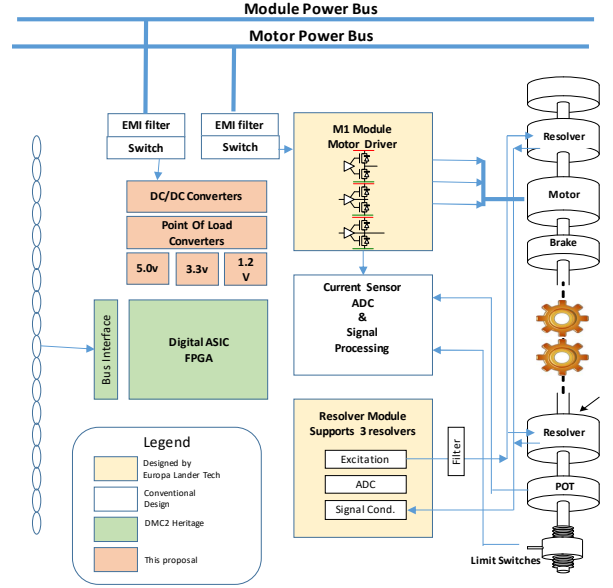

Figure 7. Current Europa Lander MCM Block Diagram, defining common SiP Modules

A. Motor Drive Module

The Motor Driver SiP MCM Module defined as "M1" provides electronics necessary to drive a 3A brushless DC motor. This SiP MCM consists of three MOSFET based half bridge drivers along with a radiation hardened MOSFET driver and its associated discrete circuitry. The M1 module was a collaborative partnership development with i3 Electronics, Binghamton NY. JPL developed and provided the electronic design, netlist and mechanical interface control document (MICD), and extreme environment electronics design principles to i3. i3 performed the detailed module design, analysis, fabrication and assembly. Assembled modules where functionally tested over standard mil-temperatures range, -65°C to +125°C. Six units were delivered and passed all preliminary tests.

The M1 assembly process chosen leverages the cold survivable chip-on-board receipt developed for the long life Mars Missions, i.e. Mars Science laboratory (MSL Rover) and currently planned M2020 Rover. M1 is BGA based Chip-on-board system using conductive and non-conductive epoxies with gold wirebonds. Figure 8 shows the M1 module configuration. The attributes: 29 x 29mm substrate (4-layer core with 3 buildup layer pairs, 12 layers total), size 21 x 21mm, 440-pin sn63 BGA array on 1.27mm pitch. The passives and half-bridge driver components were attached with conductive epoxy, non-conductive epoxy, and high silver filled adhesive for high current-carrying MOSFET die attach.
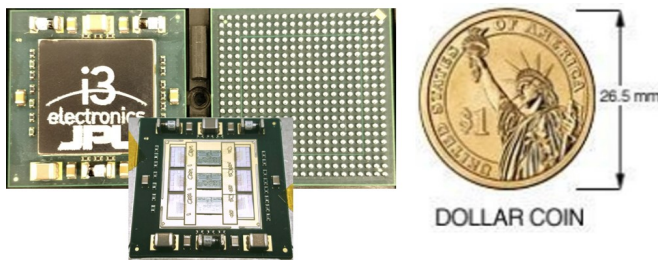
Figure 8. M1 Motor Drive Module Configuration

B. Resolver (Commutation) Module

The resolver SiP Module defined as "M3" provides electronics necessary to implement three resolver interfaces. Resolvers are used to measure position of our motors. A resolver interfaces is allocated for shaft position both before and after the gearbox. This module consists of excitation circuitry, input filter circuitry and the Analog to Digital Conversion circuitry to present the information to a FPGA for angle tracking processing. Like the M1 Module JPL developed the electronic design and breadboard prior to providing the netlist and MICD. Similar to the M1 Module, i3 also performed the detailed module design, analysis, fabrication and assembly. Delivered modules where functionally tested over standard mil-temperatures range, -65°C to +125°C. Six units delivered passed all preliminary tests.

Similar to the M1 design, material and processes leveraged the same approach. M3 is a BGA based Chip-on-board system using conductive and non-conductive epoxies with gold wirebonds. Figure 9 shows the M3 module configuration. The attributes: 35 x 35mm substrate (4-layer core with 3 buildup layer pairs, 12 layers total), size 26 x 26mm, 675-pin sn63 BGA array on 1.27mm pitch. The passives, all diodes, transistors and P-channel MOSFET driver die where attached with conductive and non-conductive epoxy.
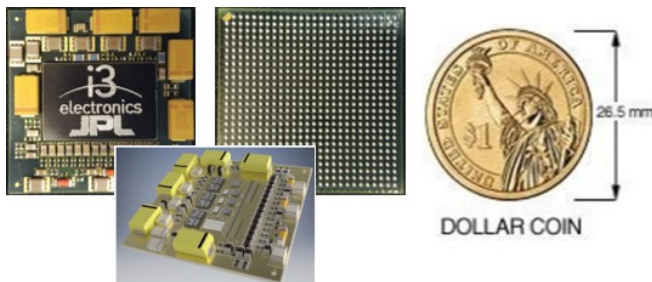

Figure 9. M3 Resolver Module Configuration

C. Point Of Load (POL) Module

The POL SiP Module defined as "POL" provides 300K radiation tolerant, dual gallium nitride (GaN) technology solution for a non-isolated Buck Converter, optimized to meet specific circuit requirements needs for the Europa Lander motor controller. This 90% efficient non-hermetic BGA reduces power consumption compared a standard linear regulator, the current state of practice for local power conversion. The small size allows its use on every board allowing a board to have power delivered at higher voltages and lower currents. This eliminates mass of connectors for power coming into the boards.
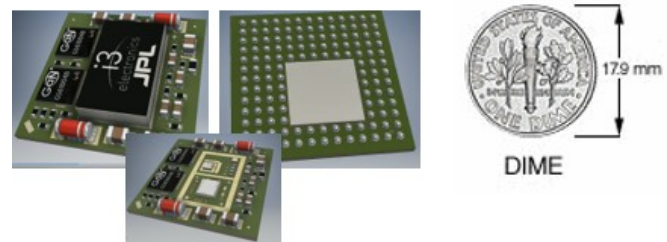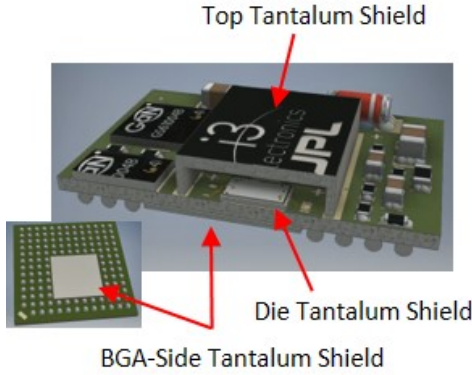

Figure 10. Point of Load Module Configuration

Similar to the M1 and M3 as far as material and processes, the POL was a BGA based Chip-on-board and Chip-Scale-Package (CSP) system using conductive and non-conductive epoxies with gold wirebonds. The major difference was the 360° radiation shielding topology. Figure 10 shows the POL module configuration. The attributes: 18 x 18mm substrate (4-layer core with 2 buildup layer pairs, 10 layers total), size 13 x 13mm, 132-pin sn63 BGA array on 1.27mm pitch. The passives, diodes die, and GaN parts where attached with conductive and non-conductive epoxy.

One of the key challenges for Europa Orbiter and Lander is procuring parts that meet the 300K radiation requirements. As an example: the Voltage regulator selected for the POL had a rating performance of only 200K rads, requiring additional radiation shielding beyond what is provide by the landed systems. Figure 11a shows the 360° shielding approach for the POL module using three tantalum elements: the BGA Shield, the Die Shield and Top Cover Shield, which seconds as a protective cover for the wirebonds during testing and handing.

The Total Ionizing Dose on Si die was evaluated with "Novice" software, performed at JPL. The analysis looked at trapped proton, trapped electron and photons. The TID was estimated inside the POL and the next assembly within the Lander, with and without tantalum shields. Figure 11b, shows the total dosage performance with and without shielding. Results show the three layer topology met the total dose radiation mission requirements.

Following the delivery and functional testing of the POL, the plan is to expose the POL Module to 300Krad dosage to validate the analysis and configuration

Figure 11. Radiation Shield Topology for the POL (a) rad shield configuration and (b) TID results for case 2 thru 4 met mission requirements.

The table in Figure 11:

	TID (krad) on Si Die in Point of Load Module										
	Case 1: No Ta, Carved CoreEZ bottom				Case2: Al-filled CoreEZ bottom				Case3: 0.125mm Ta on Co		
	Proton	Photon	Electron	subtotal	Proton	Photon	Electron	subtotal	Proton	Photon	Elec
Lander	1.32E-01	1.98E+00	4.22E+01	4.43E+01	9.83E-02	1.77E+00	3.12E+01	3.31E+01	9.62E-02	1.80E+00	2
DOV	2.09E-02	3.80E-01	6.15E+00	6.55E+00	1.78E-02	1.85E+00	5.89E+00	7.76E+00	1.64E-02	3.50E-01	5

D. Thermal Mechanical Analysis Results

Electrical, thermal and mechanical analysis were performed by i3 on the three modules: M1, M3 and POL. Electrical analysis included high current path interconnect analysis, resistance, voltage drop, and power dissipation. Thermal and mechanical analysis evaluated substrate design and processes as it affected warpage during assembly. Stress evaluated related to operational and non-operational environmental conditions such as: substrate copper balance, tensile and flexural modulus, CTE, and junction temperatures. Analysis results are shown in Table 3, indicate no issues from temperature rise, substrate warpage due to assembly process or die stresses over temperature.

Module	Substrate	Thermal			Mechanical						
						Warpage (μ)					
	Flatness (μ)	IF Temp (°C)	Tj max (°C)	Θjb (°C/W)	Ht (mm)	Mass (g)	Substrate Fab	Post Part Attach	Post Shield Attach	Effective CTE (ppm/°C)	Die Stress Principal (Mpa)
M1	5.94	50	62.87	8.56	3.86	4.53	5.94	82.71	19.51	21.2	88.34
M3	7.74	50	68.77	4.78	4.52	9.22	7.745	74.51	20.58	19.89	78.8
POL	13.845	50	80.32	12.56	3.54	2.93	13.84	14.22	32.76	22.81	55.87
PCM	in-work	50	in-work	in-work	in-work	in-work	in-work	in-work	in-work	in-work	in-work
CSM	in-work	50	in-work	in-work	in-work	in-work	in-work	in-work	in-work	in-work	in-work

Table 3: Results of Analysis

E. Dual Channel GaN Converter Module

The GaN Converter SiP Module defined, as "PCM" is a 300K radiation tolerant dual GaN non-isolated converter. Silicon based support different primary voltages and power levels while maintaining high efficiency. This fault-tolerant design allows for greater robustness for single-string applications.

Similar in construction to POL, PCM is also a BGA based Chip-on-board and Chip-Scale-Package (CSP) system using conductive and non-conductive epoxies with gold wirebonds. No radiation shielding is required; Figure 12 shows the planned PCM module configuration. The module is currently in development. The attributes: 18 x 18mm substrate (4-layer core with 2 buildup layer pairs, 10 layers total), size 13 x 13mm, 168-pin sn63 BGA array on 1.27mm pitch. The passives, diodes die, and GaN parts where attached with conductive and non-conductive epoxy.
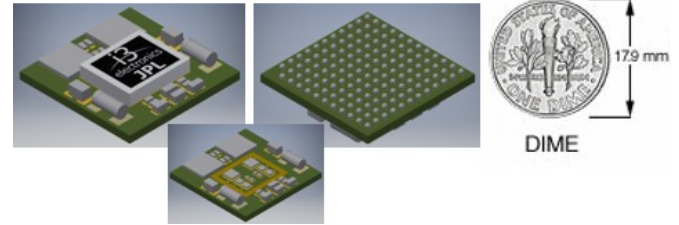

Figure 12. Dual GaN (PCM) Module Configuration

F. Current Sense Module

The Current Sense SiP Module defined as "CSM" is capable of continuously motoring phase current for motors simultaneously. There are 16 A/D channels available. 3 dedicated to current sense, 8 A/D channels for temperature sensing and 5 configurable analog inputs that allows for high common mode voltage operation.

Since the CSM effort is currently in development and the plan is to have construction similar to M3 design. BGA based Chip-on-board system using conductive and non-conductive epoxies with gold wirebonds. Figure 13 shows the proposed CSM module configuration. The attributes: 21 x 21mm substrate (4-layer core with 3 buildup layer pairs, 12 layers total), size 18 x 18mm array, 177-pin sn63 BGA array on 1.27mm pitch. Part attach process will be similar to the modules already described.

Like the PCM Module, the CSM has the same 300K radiation requirements challenges. The Linear Voltage Reference device selected for the CSM had a rating performance of only 200Krads, requiring additional radiation shielding beyond what is provide by the landed systems. The 360° shielding approach will be the same as shown in Figure 11 for the POL module, both using three tantalum elements: the BGA s Shield, the Die Shield and Top Cover Shield.
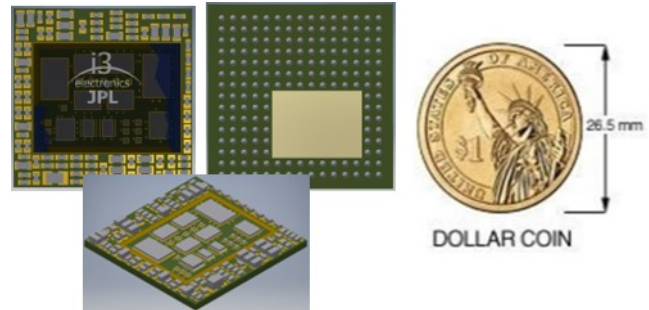

Figure 13. Proposed Current Sense Module Configuration

G. LVDS Module

To implement the internal and external SpaceWire interfaces, we are utilizing a LVDS (Low Voltage Differential Switching) module, constructed under the JPL Research and Technology - 5X Strategic Initiative effort [8]. This module implements the physical layer for the SpaceWire Interfaces. As illustrated in Figure 14, this module contain two receiver die along with two transmitter die. This component represents a 4x reduction in board area. The reduction in board area enabled by this device is key to enabling us to develop a low power COTS based computing command and data handling system for the motor drive electronics. Refer to section "G" more detail.
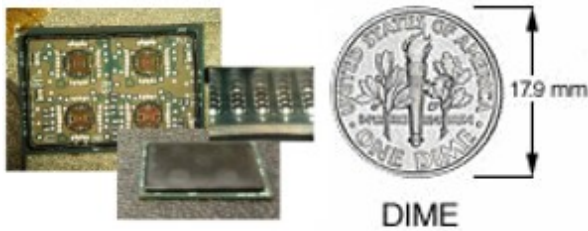

Figure 14: 16 Channel LVDS Module

To support testing, we designed and assembled a LVDS Module Test Board with custom test sockets to address yield concerns. Allows for testing the modules prior to installation onto our computer card. The card was also used to temperature test the module. We were able to test one module at a time. We found the module to work over the full operating temperature range of -55C to +125C.

H. Low Power Computing

A major development of this task is the development of single board (10cm x 10cm) Command and Data Handling System. This development started from the previously developed JPL-Sphinx development by tailoring it to meet the needs for the Europa Lander baseline computing requirements. The list that follows are key requirements for the computer card:

- The Computer Card allows for 300 Krad performance behind the 100 mils of aluminum proved by the Lander shielding allowing for an RDF of 2
- The Computer Card mass shall be less than 0.3 Kg
- The Computer Card dimensions shall fit an envelope of 100 mm x 100 mm 20 mm
- The average Computer Card power draw shall be less than 3W
- The Computer Card shall provide an EDAC protected NAND flash memory of 2 GBs for science and engineering telemetry

- The Computer Card shall be capable of interfacing with 4 cameras
- We built our design based upon the Cobham Aeroflex GR712 processor, [4] which demonstrated [9,10] our requirements where meet along with the projected power, mass and volume.

Our computer design contains all the necessary interfaces along with the computer and its associated memory. Figure 15 shows the Assembly current design, named "Manx". The Manx board is an extreme-environment-capable compute element designed for operation on the surface of Europa (300 krad TID). Is based on a dual-core LEON3FT SPARC processor, the Gaisler GR712 (datasheet). The Manx also includes a MicroSemi RTG4, radiation-hardened FPGA and supports 5 SpaceWire links, 5 motor control links, 2 UARTs, Ethernet, Camera Link (for 30fps @ 4k resolution video), GPIO, I2C, SPI, and a housekeeping suite. The RTG4 supervises the processor and provides a 50MHz clock, resets, and access to peripheral interfaces. Manx is equipped with 8GBytes of science data storage, 400MBytes of SDRAM for the processor, and dual-redundant 128KByte EEPROM devices swappable through the FPGA. Manx operates off a 5V spacecraft bus and generates internal power through on-board point-of-load regulators.
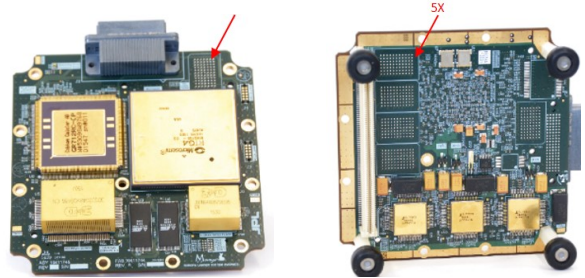

Figure 15: Manx Computer Assembly – Front side and backside (Note: arrow indicating LVDS location)

VI. LEVERAGING SYSTEM-IN-PACKAGE MODULARITY

Modularity Simplifies packaging topology. By creating a series of common custom SiP modules, allowed for a flexible approach to packaging topology and implementation. Modules can be used singly or combined as needed to create specific functionality throughout architected system. Module upgrades, replacements, or expansions are easily accomplished. Lower Costs through standardized modules, enhances the ability to either assemble a distributed or centralized system.

Baselined for the Europa Lander concept as the motor control processor, the system designers now have options to create a standalone centralized motor control 3U sized unit with individual slices to drive a single motor or several motors as shown in the block diagram in Figure 16.

As illustrated, the packaging for this motor control assembly is based upon a slice based architecture originally developed for JPL's X2000 program [9]. The design utilized modules developed under this program to construct a Motor Control Card.

This centralized modular module approach consists of our computer card along with enough Motor Control Cards necessary to control 12 motors. Each motor card can control up to three motors, with only one motor running at a time per card. Our design allows for the position of each motor to be monitored by two resolvers, one motor shaft and one on the output of the gearbox.

Each resolver module can talk to 3 resolvers. Each card has two resolver modules. Each card has 2 resolver channels per motor. One for commutation and one for output position, six channels in total. All can be running at any given time. There are four motor cards in the stack. This gives a total of 12 motors, and 24 resolver channels. In this configuration we provide the motor control and motor control computation needs for the Europa Lander.

This allowed the Europa Lander to take advantage of our potential mass and volume savings. The miniaturized motor control assembly is based upon the computer card we developed and motor control modules. Other packaging options can be entertained as shown in Figure 17, where 8 motors can be controlled in a single 6U packaging topology
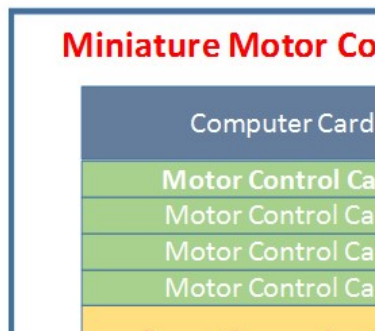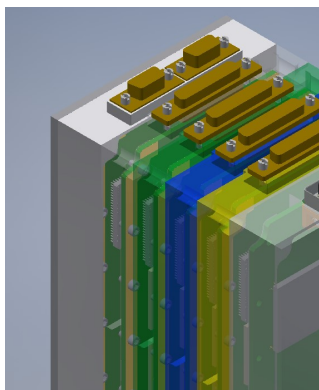

Figure 16a: Standalone Motor Control Block Diagram

Figure 16b: 3U Standalone Motor Control Module with Compute Slice, Four Motor Control Slices and Power Conversion Slice
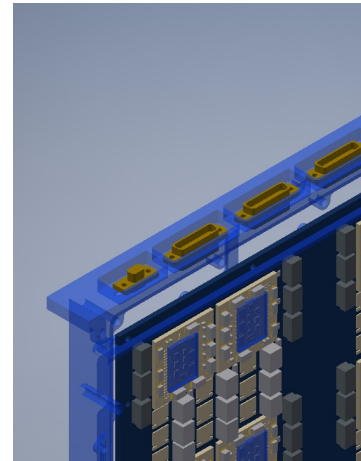

Figure 17: 6U Standalone Motor Control Module to control 8 to 12 Motors

VII. Thermal Cycling tests for Reliability

Low temperature survivability is most often determined by the environment. Survivability or cold operational electronics for these systems can lead to significant mass, power and cost savings by reducing the required active and passive thermal control, cabling and system complexity, both during cruise and after landing. Having a clear understanding of reliability and margins over the Ocean World temperature ranges and cycles have been evaluated for extreme low temperature cycling from -184°C to +85°C for 100 cycles. The margins and results on based on a 3X life margin. The work results discussed are in the following thrust areas: advanced substrate technology and low temperature part attach materials.

A. Part Attach technology

The epoxy part attach approach was based on the thermal cycle resistant electronics (TCRE) efforts at JPL qualified electrolytic Au with Au end-capped discrete parts attach using conductive and non-conductive epoxy along with Au and Al wire bonds surviving 3000 plus cycles for low temperature (-120°C to +85°C) environments using conventional polyimide substrates.

To simplify PWB fabrication of the fine features needed for mixed technology multi-chip module (MCM) solutions, ENEPIG (Electroless Ni, Electroless Pd, and Immersion Au) finish was selected because of the following attributes:

- Good planarity characteristics for attachment of ball grid array/land grid array (BGA/LGA) and elimination of black pad concerns. Additionally, the presence of palladium self-limit the gold plating thickness thereby eliminating the risk of excessive gold in the solder.

- ENEPIG simplifies the process for chip-on-board (CoB) designs allowing wire bonding, epoxy attach and solder technologies on an assembly with a single finish. Early testing using both CoreEZ and standard IPC- 4101 polyimide with ENEPIG finish and 1 mil Au wirebonds have been cycled in the following conditions: 500 thermal cycle (–55°C to 125°C), 250 thermal cycles (–130°C to 85°C) and 100 thermal cycles (-184°C to 85°C). Figure 18 shows the test vehicle and destructive pull tests resulted such that the average minus three times the standard deviation was above the 3 grams requirement.
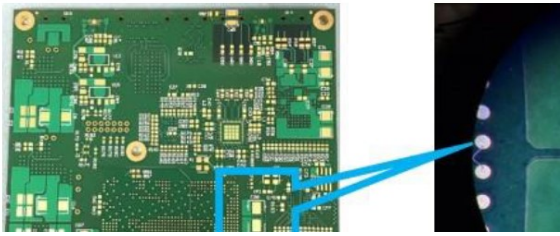

Figure 18. Photographs of the ENEPIG Wirebond Evaluation Test Vehicle

Planning for future SiP applications, i.e., part types and finishes, compatibility with substrates, required us to look at alternate conductive epoxies. The new epoxies shown in Figure 19a and 19b show material properties of epoxy candidates used with standard tin/lead parts, higher silver filled epoxies for die attach to meet higher current carrying needs and general usage epoxies for mechanical attach solutions.

Linear Material Properties

Material	Thermal Conductivity (W/mK)	Tg (°C)	T < Tg E (MPa)	T < Tg CTE (ppm/°C)	T > Tg E (MPa)	T > Tg CTE (ppm/°C)
Copper	390	NA	117000	17	NA	NA
DriClad Resin	0.35	175	7340	31	847	115
H27 Core	0.35	175	6900	24.1	2970	1.87
PSR 4000	0.23	105	2830	55	40	140
Si	145	NA	169000	3	NA	NA
63/37 Solder	48	NA	31440	24.9	NA	NA
Alumina	21	NA	303000	6	NA	NA
Tantalum	54	NA	186000	6.5	NA	NA
50/50 WCu	220	NA	180000	13	NA	NA
Epoxy Type1	1.8	110	See Chart	46	See Chart	160
Epoxy Type2	18.8	45	See Chart	47	See Chart	136
Epoxy Type3	1.59	85.7	See Chart	46.1	See Chart	160.6
Epoxy Type4	2.5	80	See Chart	31	See Chart	158

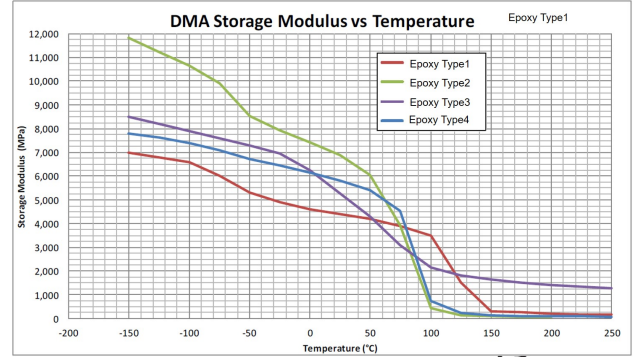**Figure 19. Future SiP MCM compatible material properties**

Figure 20 shows modulus verses temperature for the same candidates.

B. Board level interconnection reliability study on PBGAs down to cryogenic temperatures

Given the emphasis of custom SiP Module technologies needed for this effort, our first focus from a cryogenic reliability point of view was to determine performance of various Device Under Test (DUT) sizes and attach materials using a polyimide based test boards with ENEPIG finish.

The already existing solder joint thermal cycling fatigue life models are based on historical data obtained from tests done under the mil-spec temperature cycling regime and may not be effective for predicting solder join life during temperature cycling down to cryogenic temperatures. In addition, there were concerns of potential reduction of thermal cycling life of solder joints due to ductile-to-brittle transition (DBT) of solder materials [11], although the effect of DBT is more pronounced when solder joints are subjected to high deformation rate, such as shock and vibration.

The tests were done using dummy daisy chained BGA packages with comparable package size and bump pitch as the SiP modules presented in the current study. The BGA bumps were composed of Sn63 solder, and packages were attached to test boards using three different materials: Sn63 solder, 80In15Pb5Ag solder, and conductive epoxy. The reason for investigating indium solder and conductive epoxies as BGA attach materials was for potential applications where SiP modules are used in the same assembly as sensors that cannot be exposed to high reflow temperatures.

Some of the BGA assemblies were ruggedized with Parylene coating or underfill. Parylene coating has been known to extend solder joint fatigue life [12]. Underfill is widely used in flip chip, CSP, and BGA assemblies to improve solder joint fatigue life or impact reliability. 2 types of underfills were used in the current study.

	Attach material	Ruggedization	Temp cycling	BGA Package size (mm) / Pitch (mm) / QTY					
				27/1.0	15/1.0	10/0.4	13/0.4	12/0.5	7/0.5
001	Sn63	Mixed	N	3	0	0	0	0	3
002	Sn63	None	Y	3	2	1	1	1	3
003	Sn63	None	Y	3	1	1	1	1	3
004	Sn63	Parylene	Y	3	2	1	1	1	3
005	Sn63	Parylene	Y	3	1	1	1	1	3
006	Sn63	UF3811	Y	3	3	2	2	2	4
007	Sn63	SUF1589-1	Y	3	3	2	2	2	4
008	Indium	Mixed	N	3	0	0	0	0	3
009	Indium	None	Y	3	2	2	2	2	3
010	Indium	Parylene	Y	3	2	2	2	2	3
011	Indium	UF3811	Y	3	1	1	1	1	4
012	Indium	SUF1589-1	Y	3	1	1	1	1	4
013	Epoxy Type1	Mixed	N	3	0	0	0	0	3
014	Epoxy Type1	None	Y	3	2	2	2	2	3
015	Epoxy Type1	Parylene	Y	3	2	2	2	2	3
016	Epoxy Type1	Underfill 1	Y	3	1	1	1	1	4
017	Epoxy Type1	Underfill 2	Y	3	1	1	1	1	4

Table 2. Board-level reliability Test Matrix

Cold Temperature Cycling—Seventeen test vehicles were assembled using daisy chain BGAs and attached to a polyimide daisy chain test board with ENEPIG and exposed to -184°C to +85°C for 100 thermal cycles. Table 2 provides a test matrix for the thermal cycle evaluation including daisy chain BGA part information, attach material and underfill type. At this time BGAs attached with Sn63 and indium solder have completed 100 cycles. All BGAs attached with Sn63 solders have survived 100 thermal cycles. These BGAs will be tested for additional 100 cycles. For the BGAs attached with indium solder, 6 BGAs failed between 50 to 100 cycles. The 4 of the failed BGAs were the ones with largest package size, and ruggedization methods had little correlation with temperature cycling life. The lower thermal cycling life of BGA bumps attached with indium solder can be due to inherent properties of the solder joints, but also can be due to immature assembly process, as workmanship and quality often have greater impact on the reliability than inherent properties of materials. The BGA bumps in the failed parts were composed of Sn63 solder and attached with indium solder at the indium solder reflow temperature. The BGA assemblies attached with conductive epoxies are currently under test.

C. M1 and M3 Modules Exposed to Extreme Environment

Early understanding of our Custom SiP Module reliability and margins over the Europa temperature range is critical to our successes. Even though we have tested the elements that make up the SiP Modules, e.g. substrate, electronic part attach materials and Au wirebond interfaces, testing the actual Modules would provide valuable insight.

Both M1 and M3 Modules along with other test articles were delivered to Experior Laboratory in Oxnard and went through non-operational, passive low-temperature cycling, starting at +25°C to -184°C to +85°C and repeating for 100 cycles, with a ramp rate of 5°C/min. Figure 1 shows M1 and M3 in the chamber denoted by the green arrow.

After thermal cycling completed, modules were photographed using the Keyence digital microscope, followed by visual inspected using a 60X power scope. We looked for obvious failures, e.g. epoxy cracks between the aluminum shield and substrate and for epoxy separation or cracking between the electronic part end-caps to substrate. No visual evidence of cracking or separation found.

After visual inspection the module were delivered to the Europa test bed. Each module has a socketed test board, M1 was placed in the test socket and a post cycling safe-to-mate test was performed. Early results indicated there was a problem with four 100K ohm nets. The Module as removed from the socket and hand probed using a fluke meter. The four net in questions were found to read the appropriate values after several probing attempts. M1 was reinstalled into the socketed test board and M1 passed the safe to mate test, and completed the second functional phase.

The same test process/procedure was repeated for M3. The same safe-to-mate failure as was in M1 was observed. The module was probed using the same hand probing process. After probing M3 was placed back into the socketed test board and passed functional.
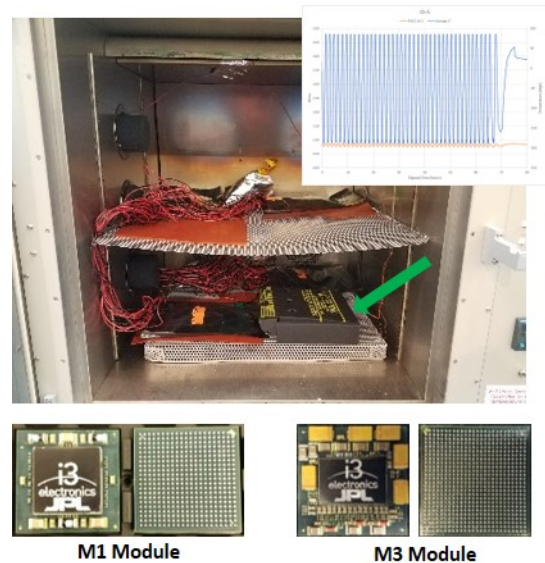

Figure 23. Photograph M1 and M3 in Thermal Cycle Chamber

VIII. SUMMARY

JPL's LDVS, Motor Driver, Resolver Modules have all been designed, built and tested over the Mil-Spec. temperature ranges. The motor control computer card has been built and tested in ambient temperatures. We have validated the M1 and M3 custom SiP modules exposed to extreme temperature environments using selected material and processes have shown to survive. These modules are

ready to be incorporated into future designs for a potential Europa Lander and other mission concepts. The only issue with respect to the computer card is the radiation, the 100Krad performance of the RTG4 FPGA and SDRAM. The RTG4 may need to be replaced with a digital ASIC. The SDRAM will need to be replaced with Rad Hard SRAM.

The balance of modules, POL, PCM and CSM are currently scheduled for fabrication and assembly in the next nine months. The potential Europa Lander delivery would include our motor control modules packaged into a motor control card / slice along with our computer card.

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